

REMARKS

Claim 27 is pending in the above-identified application. Claim 27 was rejected. With this Amendment, claim 27 was amended. Accordingly, claim 27 are at issue.

I. Objection To Drawings

The Examiner objected to Figure 15 for lacking a legend indicating that the drawings illustrate prior art. Pursuant to 37 C.F.R. § 1.121(d), enclosed is a copy of Figure 15 that has been amended to include a “Prior Art” legend. The proposed changes are to correct the drawing and do not constitute new matter. Accordingly, Applicant respectfully requests withdrawal of this objection.

II. Double Patenting Rejection of Claims

Claim 27 was rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims of U.S. Patent No. 6,677,993 in view of Akimoto et al. (U.S. Patent No. 4,942,474). In response to this objection, Applicants are submitting an appropriate Terminal Disclaimer. Accordingly, Applicants respectfully request withdrawal of this rejection.

III. 35 U.S.C. § 102 Anticipation Rejection of Claims

Claim 27 was rejected under 35 U.S.C. § 102(b) as being anticipated by *Akimoto et al.* (U.S. Patent No. 4,942,474). Applicant respectfully traverses this rejection.

Claim 27 was amended to include a horizontal scanning circuit serving as the reset element, said horizontal scanning circuit generating the reset pulse. These features are disclosed in paragraph [0035] of the specification. Thus, no new matter has been added.

Akimoto et al. is directed to a solid-state imaging device in which photoelectric conversion elements are integrated on a semiconductor substrate. The solid-state imaging device includes a plurality of photodiodes arranged in a two-dimensional matrix, amplifier means arranged in proximity to each photodiode for amplifying a signal charge stored in the photodiode, and reset means for resetting the input of the amplifier means. (col. 3, lines 38-44.) The output of the amplifier means, when the input of the amplifier means is reset and when the input is a signal charge, are separately stored in a pair of storage means. (col. 3, lines 44-49.) The output of the storage means are successively scanned by scanning means. (col. 3, lines 49-51.) The gate and drain electrodes of the reset transistor 3 are connected to a reset line 6, which is connected to the vertical scanning circuit 21. (col. 4, lines 64-67.) The storage capacitors 11, 12 are connected to a horizontal signal line 20 through horizontal gate switch transistors 13, 14, which are sequentially scanned by a horizontal scanning circuit 22. (col. 4, lines 16-21.)

Akimoto et al. does not disclose or suggest the use of a horizontal scanning circuit serving as the reset element, said horizontal scanning circuit generating the reset pulse, as recited by amended claim 27. Rather, in *Akimoto et al.*, the horizontal scanning circuit 22 affects the horizontal gate switch transistors, which operate the storage capacitors. Accordingly, Applicants respectfully submit that amended claim 27 is not anticipated by the cited art. Moreover, there is no suggestion to modify *Akimoto et al.* to utilize the horizontal scanning circuit in this way.

IV. Conclusion

In view of the above amendments and remarks, Applicant submits that all claims are clearly allowable over the cited prior art, and respectfully requests early and favorable notification to that effect.

Respectfully submitted,

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